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## PATENT ABSTRACTS OF JAPAN

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## (54) MEMORY CONTROL CIRCUIT

## (57) Abstract:

**PURPOSE:** To maximize the execution cycle of storage holding operation and to reduce energy consumption by providing a refresh means performing refresh operation in a prescribed cycle by the group of a memory cell and a means designating the refresh cycle of the memory cell group according to the shortest storage holding time.

**CONSTITUTION:** The memory control circuit is provided with a numerical registration means 300 outputting the maximum mask numerical signal corresponding to an entire storage holding operation (refresh operation) address 20 by 1:1, a storage holding operation request permission means 200 corresponding to the entire storage holding operation address 20 by 1:1, and a gate means 400 permitting the transmission of the record result of a storage holding operation request signal 10, and constructed to change the cycle performing the storage holding operation. To most of the memory cells with the storage holding ca-

capacity of more than m-times that of conventional regulation, the cycle of the storage holding operation is selectively turned to be m-times that of the prescribed regulation to omit the unnecessary storage holding operation. Thus, the energy consumption for the storage holding operation can be reduced on average since the number of the storage holding operation can be reduced as the whole.

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